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(71) Applicant *(for all designated States except US)*: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. [JP/JP]; 1006, Oaza Kadoma, Kadoma-shi, Osaka 571-8501 (JP).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: AOKI, Toru [JP/JP]; Ko 2003-51, Shimoshimayama, Saijo-shi, Ehime 793-0006 (JP).

(74) Agent: HAYASE, Kenichi; Hayase & Co. Patent Attorneys, 8F, Esaka ANA Bldg., 17-1, Enoki-cho, Suita-shi, Osaka 564-0053 (JP).

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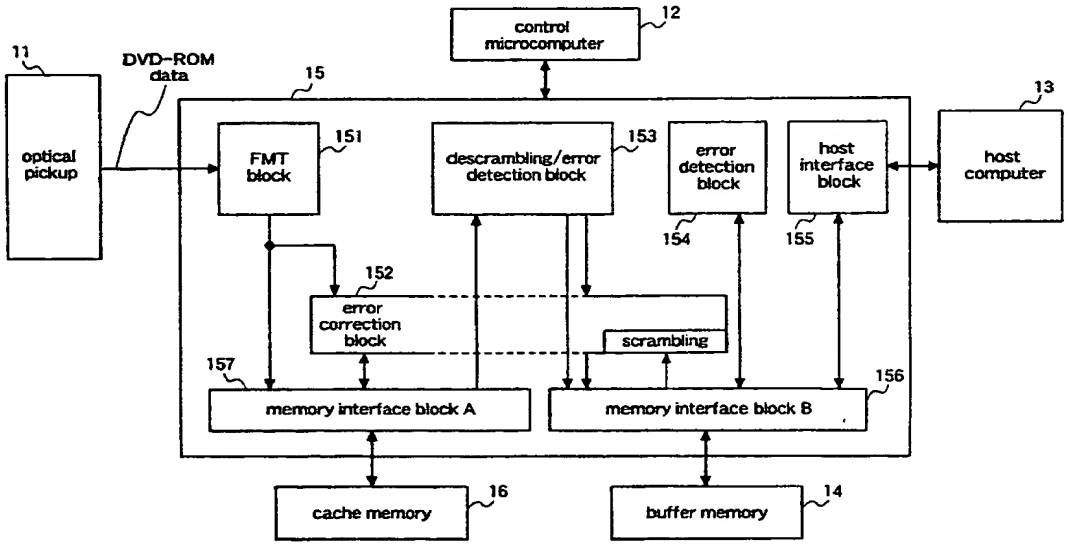
(54) Title: SIGNAL PROCESSOR FOR CORRECTING AND DETECTING ERRORS




(57) Abstract: In a signal processor according to the present invention, error correction is performed on data which has been subjected to predetermined signal processing, for each predetermined block unit, by an error correction block (152), in parallel with the operation of sequentially storing the data in a cache memory (16). Then, error detection is performed on the data for each predetermined block unit by a descrambling/error detection block (153), and the data is stored in a buffer memory (14). Based on the results of the error detection and the error correction, when there exists some error in the data, the data with the error, which is stored in the buffer memory (14), is read out to be subjected to error correction again. When there is no error, the data corresponding to one block and stored in the buffer memory (14) is transmitted to a host computer (13) without performing error correction again.

WO 01/20607 A1

DESCRIPTION

# SIGNAL PROCESSOR FOR CORRECTING AND DETECTING ERRORS

## TECHNICAL FIELD

The present invention relates to a signal processor for detecting and correcting errors in data read from a recording medium.

## BACKGROUND ART

In recent years, high quality and speedup are demanded of a DVD-ROM, which has become widespread as a digital memory, to increase the reliability of data read from a DVD disk. With the demand, a signal processor for correcting errors in the disk is required to have rapid processing means, and it is aimed at realization of high-speed data processing.

A conventional CD-ROM signal processor performs error correction by a predetermined number of times. Further, the CD-ROM signal processor writes inputted data in a buffer memory and, simultaneously, detects errors in the data by using CRC (Cyclic Redundancy Check). Based on the result of CRC, when the data is decided as "error-free data", the signal processor reduces the predetermined number of error corrections.

In the case of DVD-ROM data, however, since inputted data

is not previously subjected to error correction in contrast to the CD-ROM data, the error rate is higher in the DVD-ROM data than in the CD-ROM data. Therefore, when the DVD-ROM data is subjected to CRC, the result of CRC is, in most cases, that there are errors in the DVD-ROM data.

Figure 6 is a block diagram illustrating the structure of a conventional DVD-ROM signal processor.

In figure 6, a DVD-ROM signal processor 65 receives DVD-ROM digital signal data (hereinafter referred to as "data") which is read by an optical pickup 61, and outputs the data after error correction to a host computer 63. The DVD-ROM signal processor 65 is under control of a control microcomputer 62, and is connected with a buffer memory 64 which stores data.

To be specific, the DVD-ROM signal processor 65 is provided with an FMT block 651 for capturing the DVD-ROM data outputted from the optical pickup 61, and storing it in the buffer memory 64; an error correction block 652 for correcting errors in the data stored in the buffer memory 64; a descrambling block 653 for descrambling the scrambled data; an error detection block 654 for detecting errors in the data after error correction, which data is stored in the buffer memory 64; a host interface block 655 for transmitting error-free data to the host computer, based on the result of the error detection by the error detection block 654; and a memory

interface block 656 for controlling the processing between the DVD-ROM signal processor 65 and the buffer memory 64.

The operation of the conventional DVD-ROM signal processor so constructed will be described with reference to figures 4 and 6.

Figure 4 is a diagram illustrating the data format constituting one ECC block.

As shown in figure 4, the logical format of the DVD-ROM data outputted from the optical pickup 61 is constituted with 182×208 bytes as one ECC (Error Correcting Code) block.

First of all, the data read by the optical pickup 61 forms one component unit with 182 bytes as a C1 code word. The C1 code word is composed of 172 bytes of user data and 10 bytes of C1 parity. One ECC block is composed of plural C1 code words and plural C2 code words, each C2 code word comprising 208 bytes obtained by collecting one byte from each C1 code word. Each C2 code word is composed of 192 bytes of user data and 16 bytes of C2 parity. The DVD-ROM data has been scrambled in advance.

In figure 6, the FMT block 651 converts the DVD-ROM serial data outputted from the optical pickup 61 into parallel data (serial to parallel conversion), subjects the converted data to demodulation and sync detection, and writes the parallel data in the buffer memory 64 through the memory interface block 656.

The error correction block 652 reads the DVD-ROM data written in the buffer memory 64, through the memory interface block 656, performs syndrome calculation on the C1 code words and the C2 code words shown in figure 4, and calculates the error position and the error pattern by using the result of the syndrome calculation. Based on the result of the syndrome calculation, the error correction block 652 terminates the error correction when the data has no error. However, when the data has some error, the error correction block 652 reads the error data stored in the buffer memory 64, through the memory interface block 656, performs error correction on the error data, and writes the corrected data over the address of the error data stored in the buffer memory 64, through the memory interface block 656.

The descrambling block 653 reads the DVD-ROM data which has been subjected to error correction and is stored in the buffer memory 64, through the memory interface block 656, descrambles the data according to a predetermined method, and writes the data in the buffer memory 64 through the memory interface block 656.

The error detection block 654 reads the DVD-ROM data which has been descrambled and is stored in the buffer memory 64, through the memory interface block 656, and detects errors in the read data by performing predetermined calculation.

The host interface block 655 transmits, to the host

computer 63, the DVD-ROM data which has been decided as "error-free data" in both of the error correction block 652 and the error detection block 654.

Each of the above-mentioned blocks is constructed so as to operate at a predetermined timing according to an instruction from the control microcomputer 62.

In the conventional DVD-ROM signal processor, however, when the DVD-ROM data is subjected to error correction, the following operations are performed on the buffer memory 64: writing of data from the FMT block 651, reading and writing of data from the error correction block 652, reading and writing of data from the descrambling block 653, reading of data from the error detection block 654, and reading of data from the host interface block 655. That is, since reading and writing of data are performed frequently through the buffer memory 64, the memory band width is pressed and, therefore, the signal processor cannot perform high-speed access and higher-speed data processing.

The present invention is made to solve the above-described problem, and it is an object of the present invention to provide a signal processor which can reduce the number of memory accesses by reducing the number of error corrections, thereby realizing higher-speed data processing.

## DISCLOSURE OF THE INVENTION

A signal processor according to the present invention (Claim 1) is a signal processor for subjecting data read from a recording medium to predetermined digital signal processing, and subjecting the data, which has been subjected to the predetermined digital signal processing, to error correction for each predetermined error correction block. This signal processor comprises: memory means for sequentially storing the data which has been subjected to the predetermined digital signal processing; error correction means for subjecting the data, which has been subjected to the predetermined digital signal processing, to error correction for each predetermined error correction block; descrambling/error detection means for descrambling the data which has been subjected to the error correction, and detecting errors in the data after the descrambling; and control means for transmitting error-free data to a display unit when there is no error in the data which has been subjected to the error detection.

In the signal processor so constructed, the number of data error corrections can be reduced, whereby reduced power consumption of the device itself can be achieved. Further, since the number of memory accesses to the memory means for error correction can be reduced, the access right to the memory means can be assigned to another block, whereby high-speed processing of the signal processor is realized.

According to the present invention (Claim 2), in the

signal processor described in Claim 1, the error correction means comprises: a syndrome calculator for calculating syndrome of the data which has been subjected to the predetermined digital signal processing; an error position/pattern calculator for calculating the error position and the error pattern after the syndrome calculation; error correction result holding means for holding information as to whether the data detected by the error position/pattern calculator is error-correctable or not; data correction means for correcting errors in the data on the basis of the result of the syndrome calculation; and number-of-error-correction control means for controlling the number of error corrections.

In the signal processor so constructed, the time required for memory access to the memory means can be reduced by reducing the number of error corrections and, furthermore, speedup of data processing is achieved.

According to the present invention (Claim 3), in the signal processor described in Claim 1, the descrambling/error detection means comprises: descrambling means for descrambling the data which has been corrected by the error correction means; error detection means for detecting errors in the descrambled data; and error detection result holding means for holding the result of the error detection as to whether there is any error in the data which has been subjected to the error detection.

In the signal processor so constructed, based on the result of error detection, when there is no error, the data is transmitted to the host computer without performing error correction again, whereby the number of error corrections can be reduced. Accordingly, the power consumption of the device itself can be reduced.

According to the present invention (Claim 4), in the signal processor described in Claim 1, the data subjected to the predetermined digital signal processing is read from the memory means for each predetermined error correction block, followed by error detection and error correction; when there is some error, the error is corrected by the error correction means for each predetermined error correction block; when there is no error, the data is transmitted to the display means for each predetermined error correction block.

In the signal processor so constructed, the time required for memory access to the memory means can be reduced by terminating the second and more error corrections or reducing the number of error corrections for the data in each predetermined error correction block stored in the memory means, and further high-speed transmission of the data to the host computer is achieved.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram illustrating the structure of

a DVD-ROM signal processor according to a first embodiment of the present invention.

Figure 2 is a block diagram illustrating the internal structure of an error correction block according to a second embodiment of the present invention.

Figure 3 is a block diagram illustrating the internal structure of a descrambling/error detection block according to a third embodiment of the present invention.

Figure 4 is a diagram illustrating the data format constituting one ECC block.

Figure 5 is a timing chart of memory access in DVD-ROM signal processing according to a fourth embodiment.

Figure 6 is a block diagram illustrating the structure of the conventional DVD-ROM signal processor.

BEST MODE TO EXECUTE THE INVENTION

**Embodiment 1.**

Figure 1 is a block diagram illustrating the structure of a DVD-ROM signal processor according to a first embodiment of the present invention.

In figure 1, a DVD-ROM signal processor 15 receives DVD-ROM digital signal data (hereinafter referred to as "data") which is read by an optical pickup 11, and outputs the data after error correction to a host computer 13. The DVD-ROM signal processor 15 is controlled by a control microprocessor

12, and it connects a cache memory 16 for storing the data and to a buffer memory for storing the data stored in the cache memory 16.

To be specific, the DVD-ROM signal processor 15 is provided with an FMT block 151 for capturing the DVD-ROM data outputted from the optical pickup 11; an error correction block 152 for correcting errors in the data stored in the cache memory 16 and the buffer memory 14; a descrambling/error detection block 153 for descrambling the scrambled data, and detecting errors in the descrambled data; an error detection block 154 for detecting errors in the data which has been subjected to error correction and is stored in the buffer memory 14; a host interface block 155 for transmitting error-free data to the host computer 13, based on the result of error detection by the error detection block 154; a memory interface block B 156 for controlling the processing between the DVD-ROM signal processor 15 and the buffer memory 14; and a memory interface block A 157 for controlling the processing between the DVD-ROM signal processor 15 and the cache memory 16.

The operation of the signal processor so constructed will be described with reference to figures 1 and 4.

Figure 4 is a diagram illustrating the data format constituting one ECC block.

As shown in figure 4, the logical format of the DVD-ROM

data outputted from the optical pickup 11 is constituted with 182×208 bytes as one ECC block.

First of all, the data read by the optical pickup 11 forms one component unit with 182 bytes as a C1 code word. The C1 code word is composed of 172 bytes of user data and 10 bytes of C1 parity. One ECC block is composed of plural C1 code words and plural C2 code words, each C2 code word having 208 bytes obtained by collecting one byte from each C1 code word. Each C2 code word is composed of 192 bytes of user data and 16 bytes of C2 parity. The DVD-ROM data has been scrambled in advance.

Initially, with reference to figure 1, the DVD-ROM data outputted from the optical pickup 11 is converted from serial data to parallel data (serial to parallel conversion) by the FMT block 151. The parallel data are subjected to demodulation and sync detection, and one of the parallel data is written in the cache memory through the memory interface block A 157. At the same time, the other one of the parallel data is transmitted for each ECC block to the error correction block 152, wherein it is subjected to error correction. The data which has been subjected to error correction by the error correction block 152 is written in the cache memory 16 through the memory interface block A 157.

Next, the data after error correction is read from the cache memory 16 through the memory interface block A 157, and

the scrambled data is subjected to descrambling and error correction by the descrambling/error detection block 153, and the data is transmitted to the buffer memory 14 through the memory interface block B 156. At this time, when the descrambling/error detection block 153 detects some error in the data, error correction is carried out again by the error correction block 152.

The data which has been subjected to error correction by the error correction block 152 is inputted to the error detection block 154 through the buffer memory 14 and the memory interface block B 156, wherein error detection is carried out again. Based on the result of the error detection, only the data decided as "error-free data" is transmitted to the host computer 13 through the host interface block 155.

As described above, in the signal processor according to the first embodiment, the DVD-ROM data inputted to the signal processor is subjected to error detection and error correction for every ECC block. When the data has some error, the data is subjected to error correction for every ECC block. When the data has no error, the data is transmitted to the host computer 13 for every ECC block. Therefore, although in the conventional example error correction is carried out by a predetermined number of times, such wasteful correction work is avoided, and the number of error corrections is reduced. Accordingly, it is possible to reduce the power consumption of

the device itself. Further, since the number of memory accesses to the buffer memory 14 for error correction is reduced, the access right to the buffer memory 14 can be assigned to another block, whereby speedup of the signal processor is realized.

**Embodiment 2.**

Figure 2 is a block diagram illustrating the internal structure of an error correction block according to a second embodiment of the present invention.

With reference to figure 2, an error correction block 152 is provided with a syndrome calculator 1521 for performing syndrome calculation; a scrambling circuit 1522 for scrambling descrambled data; an error position/pattern calculation block 1523 for calculating the error position in data and the error pattern on the basis of the result from the syndrome calculator 1521, and detecting data having uncorrectable errors (hereinafter referred to as "error uncorrectable data"); an error correction result holding circuit 1524 for holding information as to whether there is error uncorrectable data or not, which is detected in the error position/pattern calculation block 1523; data correction circuit 1525 for correcting errors in the data according to the error position and the error pattern calculated from the syndrome by the error position/pattern calculation block 1523; and a number-of-error-correction control circuit 1526 for controlling the

number of error corrections.

The operation of the error correction block so constructed will be described with reference to figure 2.

Initially, in the above-described first embodiment, the DVD-ROM data transmitted to the error correction block 152 is inputted to the syndrome calculator 1521 for each ECC block, wherein the data is subjected to syndrome calculation. At this time, if there is some error at the point of time when 182 bytes of data equivalent to the C1 code word have been inputted, the result of the syndrome calculation is transmitted to the error position/pattern calculation block 1523, wherein the error position and the error pattern are calculated.

In the error position/pattern calculation block 1523, it is detected whether there is any uncorrectable error or not, and the information about the presence or absence of uncorrectable error is stored in the error correction result holding circuit 1524. The information about the presence or absence of uncorrectable error, which is stored in the error correction result holding circuit 1524, is output to the number-of-error-correction control circuit 1526.

On the other hand, the information about the error position and the error pattern calculated in the error position/pattern calculation block 1523 is transmitted to the data correction circuit 1525. The data correction circuit 1525

reads the data stored in the address indicated by the error position from the cache memory 16 through the memory interface block A 157, and performs error correction by using the error position and the error pattern calculated by the error position/pattern calculation block 1523. The data which has been subjected to error correction by the data correction circuit 1525 is written in the address indicating the error position which is stored in the cache memory, through the memory interface block A 157.

The data which has been subjected to the first error correction in this way is subjected to error detection in the descrambling/error detection block 153, and transmitted to the buffer memory 14 through the memory interface block B. At this time, when some error is detected in the descrambling/error detection block 153, error correction is again carried out in the error correction block 152. Hereinafter, this process will be described in more detail.

In figure 2, the number-of-error-correction control circuit 1526 decides whether there is any error in the data stored in the buffer memory 14, on the basis of the information from the error correction result holding circuit 1524 and the descrambling/error detection block 153 shown in figure 1. Based on the result of the detection, when there is no error, the number-of-error-correction control circuit 1526 outputs the status of "free from error" to the control

microcomputer 12. However, when there is some error in the data stored in the buffer memory 14, the number-of-error-correction control circuit 1526 outputs the status of "error" to the control microcomputer 12, and the syndrome calculator 1521 performs syndrome calculation again.

The syndrome calculator 1521 reads the data with error stored in the buffer memory 14, through the memory interface block B 156. The read data is initially subjected to scrambling by the scrambling circuit 1522, and then converted to the data that can be subjected to syndrome calculation. The converted data is inputted to the syndrome calculator 1521 for each ECC block, and subjected to syndrome calculation. If there is some error at the point of time when 182 bytes of data equivalent to the C1 code word or 208 bytes of data equivalent to the C2 code word have been inputted, the result of the syndrome calculation is transmitted to the error position/pattern calculation block 1523, wherein the error position and the error pattern are calculated.

Next, the information about the calculated error position and error pattern is transmitted to the data correction circuit 1525. The data correction circuit 1525 reads the data in the address indicating the error position from the buffer memory 14 through the memory interface block B156, and performs error correction by using the error position and the error pattern calculated by the error position/pattern

calculation block 1523. Then, the data which have been subjected to error correction in the data error correction circuit 1525 is written in the address indicating the error position of the data stored in the buffer memory 14, through the memory interface block B156.

As described above, in the signal processor according to the second embodiment, syndrome calculation is performed on the data of each ECC block unit, which is inputted to the error correction block 152, and then error correction is performed on the data of each ECC block unit according to the result of the calculation. Therefore, the number of error corrections can be reduced and, furthermore, the number of memory accesses to the memory means can be reduced. Accordingly, high-speed data processing can be achieved.

**Embodiment 3.**

Figure 3 is a block diagram illustrating the internal structure of a descrambling/error detection block according to a third embodiment of the present invention.

In figure 3, a descrambling/error detection block 153 is provided with a descrambling circuit 1531 for descrambling scrambled data; an error detection circuit 1532 for detecting errors in the descrambled data; and an error detection result holding circuit 1533 for holding the result of error detection (presence or absence of error) by the error detection circuit 1532.

The operation of the descrambling/error detection block so constructed will be described with reference to figure 3.

Initially, the data which has been subjected to error correction in the error correction block 152 is inputted to the descrambling circuit 1531 from the cache memory 16 through the memory interface block A 157, and the data is descrambled according to a predetermined method. The descrambled data is transmitted to the error detection circuit 1532, wherein errors in the data are detected by predetermined calculation. The data after the error detection is transmitted to the buffer memory 14 through the memory interface block B156. Further, information about the result of the error detection by the error detection circuit 1532 is latched in the error detection result holding circuit 1533, and then outputted to the number-of-error-correction control circuit 1526 (see figure 2) in the error correction block 152.

As described above, in the signal processor according to the third embodiment, the inputted data is descrambled and then subjected to error detection. Based on the result of the error detection, when there is no error, the data is transmitted to the host computer without performing data correction again. Therefore, the number of error corrections can be reduced, resulting in reduced power consumption of the signal processor.

**Embodiment 4.**

Figure 5 is a timing chart of memory access of a DVD-ROM signal processor according to a fourth embodiment of the present invention.

First of all, each of codes shown in figure 5 will be described.

N~N+3 denote block numbers of blocks when the data inputted to the DVD-ROM signal processor is subjected to error correction for each ECC block.

Process 1 denotes the process from when the data inputted to the DVD-ROM signal processor is inputted to the cache memory 16 and the error correction block 152 through the FMT block 151 to when the first error correction is carried out.

Process 2 denotes the process of performing the second and further error correction in the error correction block 152 when the data has some error in Process 1.

Process 3 denotes the process of transmitting error-free data to the host computer 13 through the host interface block 155 when the data has no error.

The operation of the DVD-ROM signal processor so constructed will be described with respect to the timing of memory access, with reference to figure 5.

In figure 5, for example, the data corresponding to the Nth, (N+2)th, and (N+3)th blocks are constituted by the error-free or error correctable C1 code word while the data corresponding to the (N+1)th block includes the error

uncorrectable C1 code word.

Initially, with respect to the data in the Nth, (N+2)th, and (N+3)th blocks, these data having no errors at the point of time when Process 1 is ended are stored in the buffer memory 14. In this case, Process 1 is not followed by Process 2 but followed by Process 3 wherein the error-free data are transmitted for each ECC block to the host computer 13.

On the other hand, with respect to the data in the (N+1)th block, since this data has an error at the point of time when Process 1 is ended, Process 1 is followed by Process 2 wherein the error data is corrected. Those blocks containing the data which are finally decided as "error-free error" are transmitted to the host computer 13 in Process 3.

As described above, according to the signal processor of this fourth embodiment, the DVD-ROM data inputted to the signal processor is processed for every ECC block from when capture of the data is started to when the data is transmitted to the host computer 13. Therefore, in the case where Process 1 is performed on the data corresponding to one ECC block and then Process 3 is performed without performing Process 2 because there is no error, the access time inside the signal processor can be reduced by one ECC block. Accordingly, high-speed transmission of the data to the host computer 13 is realized.

APPLICABILITY IN INDISTORY

As described above, the signal processor according to the present invention can reduce the number of memory accesses by reducing the number of error corrections to process data at higher speed. Especially, it is suitable as a signal processor for which speedup is demanded, such as a DVD-ROM.

CLAIMS

1. A signal processor for subjecting data read from a recording medium to predetermined digital signal processing, and subjecting the data, which has been subjected to the predetermined digital signal processing, to error correction for each predetermined error correction block, said signal processor comprising:

memory means for sequentially storing the data which has been subjected to the predetermined digital signal processing;

error correction means for subjecting the data, which has been subjected to the predetermined digital signal processing, to error correction for each predetermined error correction block;

descrambling/error detection means for descrambling the data which has been subjected to the error correction, and detecting errors in the data after the descrambling; and

control means for transmitting error-free data to a display unit when there is no error in the data which has been subjected to the error detection.

2. A signal processor as described in Claim 1 wherein said error correction means comprises:

a syndrome calculator for calculating syndrome of the data which has been subjected to the predetermined digital signal

processing;

an error position/pattern calculator for calculating the error position and the error pattern after the syndrome calculation;

error correction result holding means for holding information as to whether the data detected by the error position/pattern calculator is error-correctable or not;

data correction means for correcting errors in the data on the basis of the result of the syndrome calculation; and

number-of-error-correction control means for controlling the number of error corrections.

3. A signal processor as described in Claim 1 wherein said descrambling/error detection means comprises:

descrambling means for descrambling the data which has been corrected by the error correction means;

error detection means for detecting errors in the descrambled data; and

error detection result holding means for holding the result of the error detection as to whether there is any error in the data which has been subjected to the error detection.

4. A signal processor as described in Claim 1 wherein:

the data subjected to the predetermined digital signal processing is read from the memory means for each

predetermined error correction block, followed by error detection and error correction;

when there is some error, the error is corrected by the error correction means for each predetermined error correction block;

when there is no error, the data is transmitted to the display means for each predetermined error correction block.

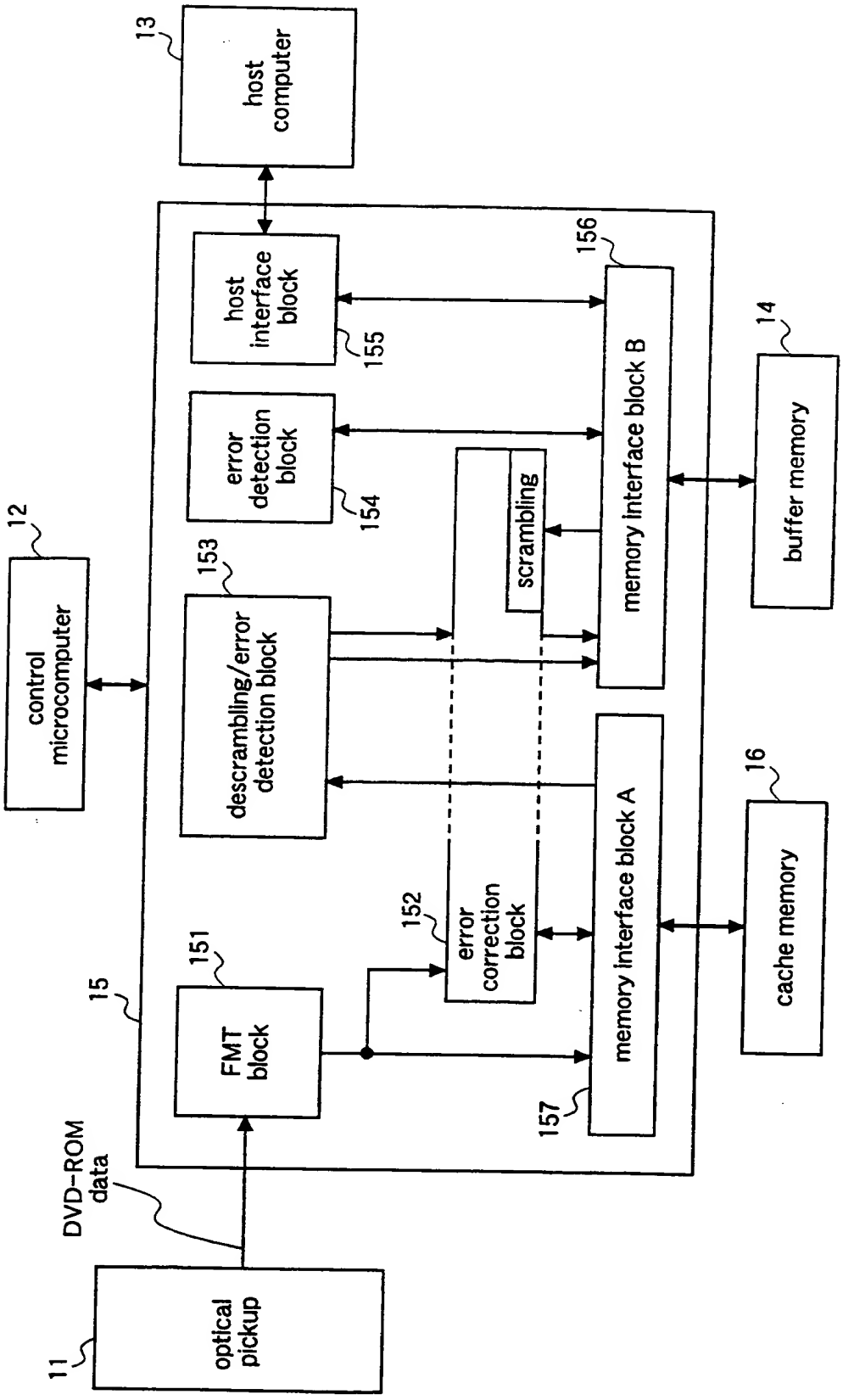

13
host computer
host interface block
155
156
memory interface block B
14
buffer memory
error detection block
154
scrambling
12
control microcomputer
153
descrambling/error detection block
152
error correction block
151
FMT block
15
memory interface block A
157
16
cache memory
DVD-ROM data
optical pickup
11

Fig.1

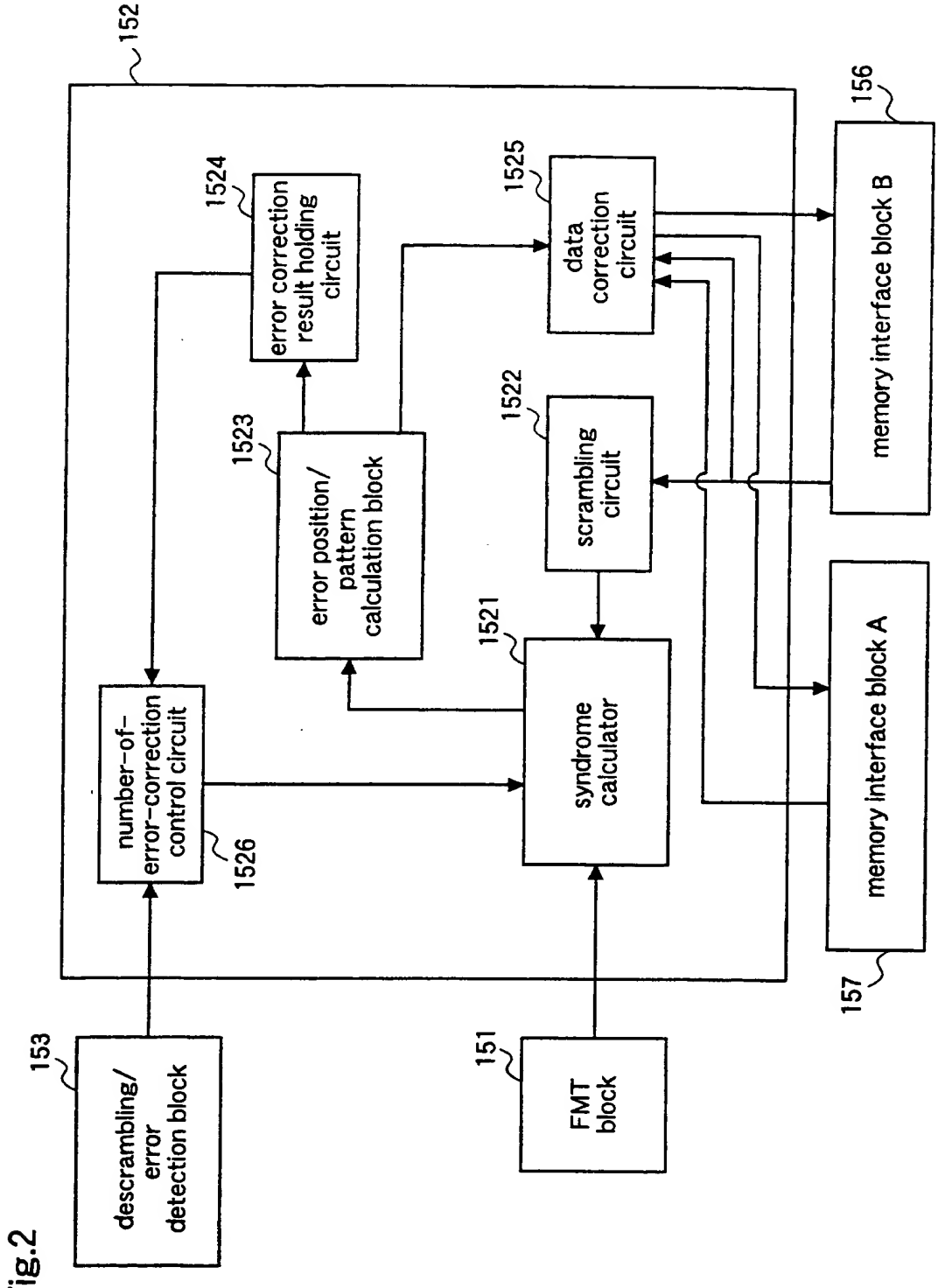

152
156
1524
error correction result holding circuit
1525
data correction circuit
memory interface block B
1523
error position/ pattern calculation block
1522
scrambling circuit
1521
syndrome calculator
number-of-error-correction control circuit
1526
memory interface block A
157
153
descrambling/ error detection block
151
FMT block

Fig.2

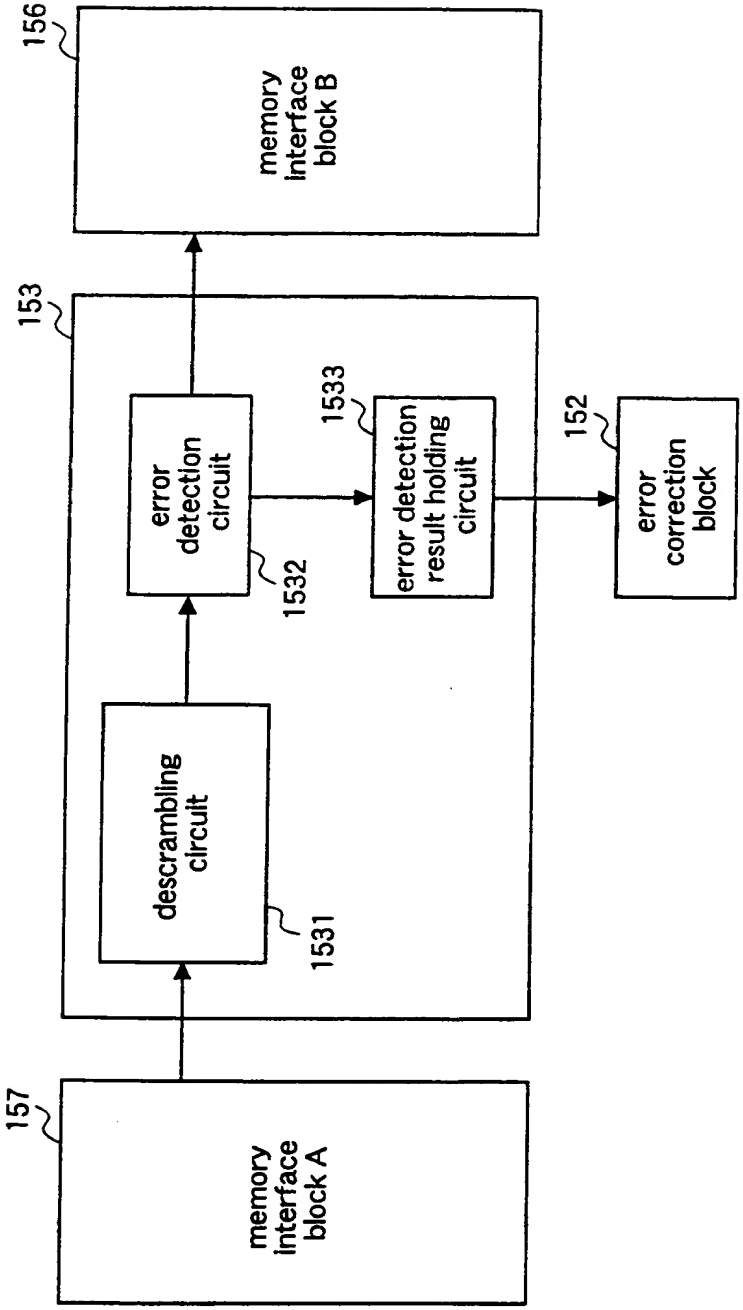

156
memory interface block B
153
error detection circuit
1533
error detection result holding circuit
152
error correction block
1532
descrambling circuit
1531
157
memory interface block A

Fig.3

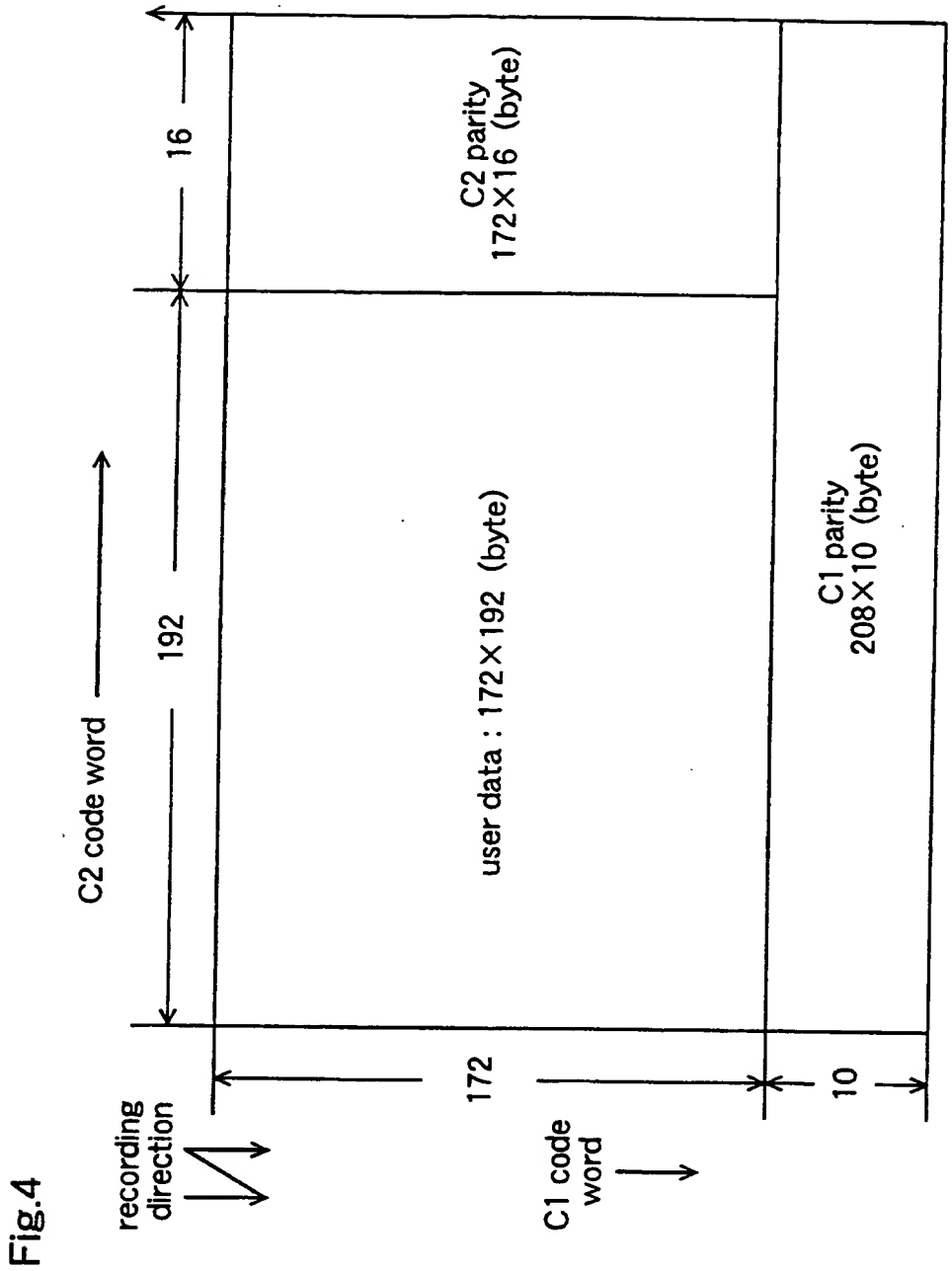

C2 parity
172×16 (byte)
16
192
C2 code word
user data : 172×192 (byte)
C1 parity
208×10 (byte)
172
10
recording direction
C1 code word

Fig.4

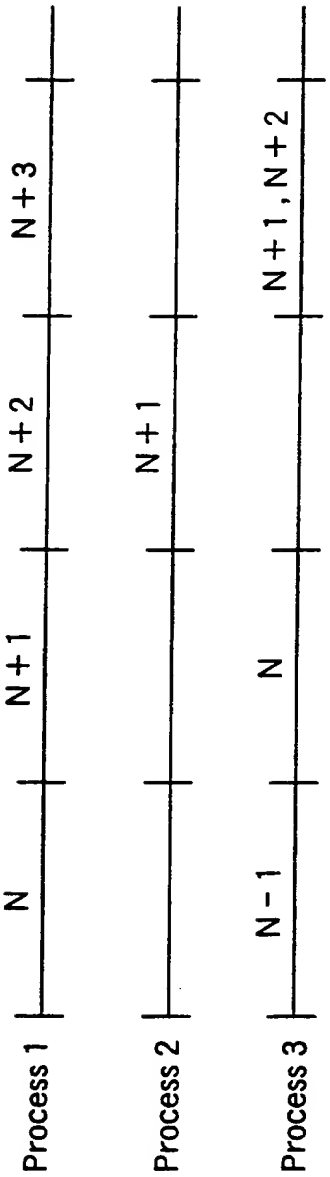



Fig.5

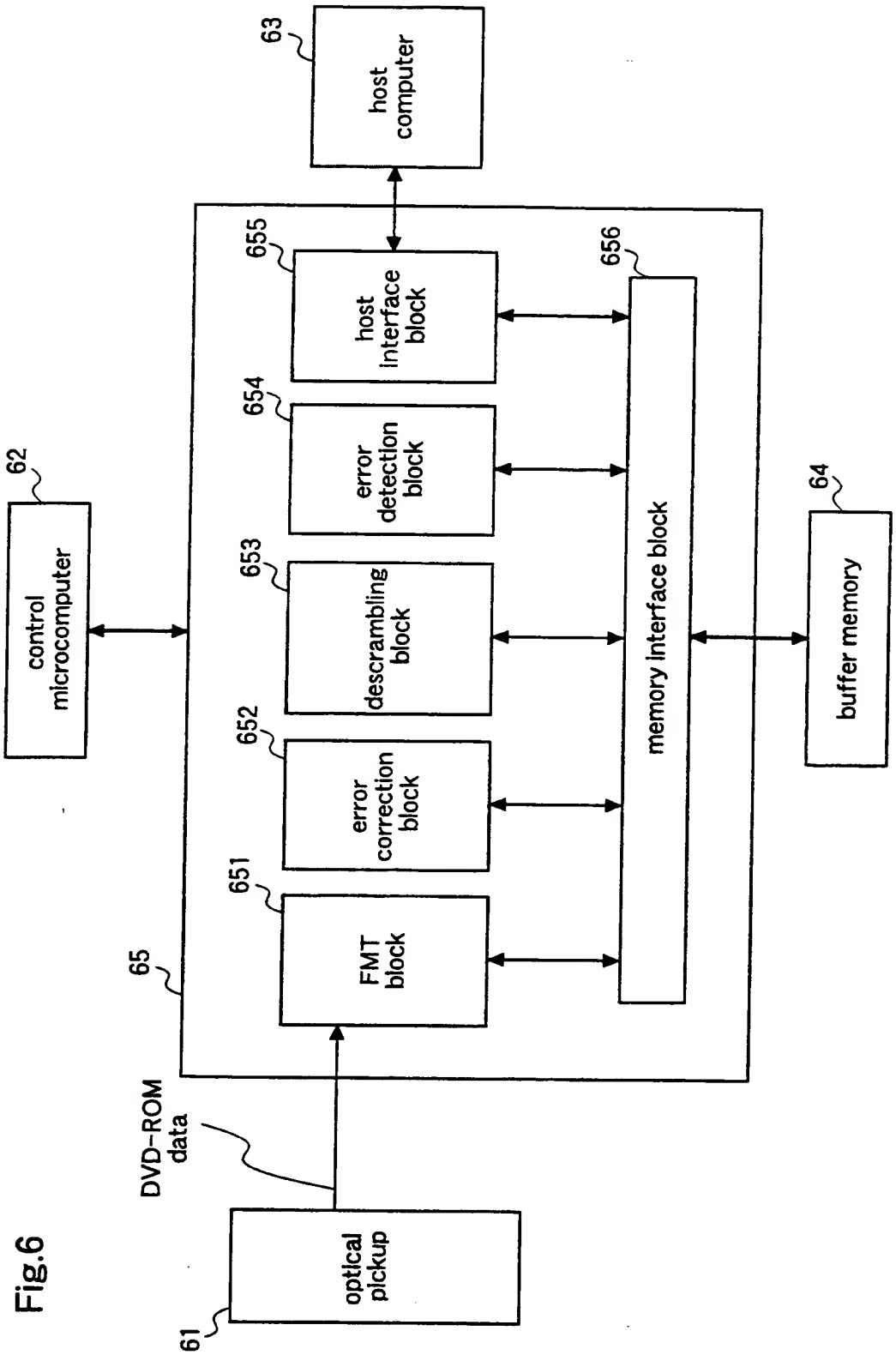

63
host computer
655
host interface block
656
654
error detection block
62
control microcomputer
653
descrambling block
memory interface block
64
buffer memory
652
error correction block
651
FMT block
65
DVD-ROM data
optical pickup
61

Fig.6

# INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/JP 00/06122

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11B20/18 H03M13/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11B H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A,P | US 6 003 151 A (CHUANG CHENG-TE)<br>14 December 1999 (1999-12-14)<br>abstract; figures 1,6,7<br>column 1, line 61 -column 4, line 19<br>column 5, line 51 -column 6, line 31<br>column 10, line 6 -column 12, line 24<br>column 15, line 3 - line 19 | 1-4 |
| A | PATENT ABSTRACTS OF JAPAN<br>vol. 1998, no. 10,<br>31 August 1998 (1998-08-31)<br>& JP 10 126279 A (MATSUSHITA ELECTRIC IND CO LTD), 15 May 1998 (1998-05-15)<br>abstract | 1,2 |

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 27 November 2000 | 04/12/2000 |

| Name and mailing address of the ISA | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL – 2280 HV Rijswijk<br>Tel. (+31–70) 340–2040, Tx. 31 651 epo nl,<br>Fax: (+31–70) 340–3016 | Schiwy-Rausch, G |

1

Form PCT/ISA/210 (second sheet) (July 1992)

# INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/JP 00/06122

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication,where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | PATENT ABSTRACTS OF JAPAN<br>vol. 1997, no. 08,<br>29 August 1997 (1997-08-29)<br>& JP 09 091889 A (MATSUSHITA ELECTRIC IND CO LTD); 4 April 1997 (1997-04-04)<br>abstract | 1-3 |
| A | EP 0 939 403 A (MATSUSHITA ELECTRIC IND CO LTD) 1 September 1999 (1999-09-01)<br>column 2, line 16 - line 47<br>column 3, line 3 - line 33<br>column 17, line 17 -column 20, line 35<br>figures 4-8 | 1,2 |
| A | PATENT ABSTRACTS OF JAPAN<br>vol. 1997, no. 09,<br>30 September 1997 (1997-09-30)<br>& JP 09 139026 A (MITSUBISHI ELECTRIC CORP), 27 May 1997 (1997-05-27)<br>abstract | 1,4 |
| A | PATENT ABSTRACTS OF JAPAN<br>vol. 1999, no. 11,<br>30 September 1999 (1999-09-30)<br>& JP 11 168392 A (TOSHIBA CORP),<br>22 June 1999 (1999-06-22) | |

1

# INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter. ...nal Application No
PCT/JP 00/06122

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| US 6003151 A | 14-12-1999 | NONE | |
| JP 10126279 A | 15-05-1998 | NONE | |
| JP 09091889 A | 04-04-1997 | NONE | |
| EP 0939403 A | 01-09-1999 | CN 1233053 A<br>JP 11338723 A | 27-10-1999<br>10-12-1999 |
| JP 09139026 A | 27-05-1997 | NONE | |
| JP 11168392 A | 22-06-1999 | NONE | |

PATENT COOPERATION TREATY

# PCT

## INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

| Applicant's or agent's file reference | **FOR FURTHER ACTION** see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below. | |
|---|---|---|
| P23070-PO | | |
| International application No. | International filing date *(day/month/year)* | (Earliest) Priority Date *(day/month/year)* |
| PCT/JP 00/06122 | 08/09/2000 | 10/09/1999 |
| Applicant | | |
| MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. et al. | | |

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 4 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language,** the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

[ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

[ ] contained in the international application in written form.

[ ] filed together with the international application in computer readable form.

[ ] furnished subsequently to this Authority in written form.

[ ] furnished subsequently to this Authority in computer readble form.

[ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

[ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

[ ] the text is approved as submitted by the applicant.

[X] the text has been established by this Authority to read as follows:

SIGNAL PROCESSIR FOR CORRECTING AND DETECTING ERRORS

5. With regard to the **abstract,**

[ ] the text is approved as submitted by the applicant.

[X] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 1

[X] as suggested by the applicant.

[ ] None of the figures.

[ ] because the applicant failed to suggest a figure.

[ ] because this figure better characterizes the invention.

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP 00/06122

**Box III TEXT OF THE ABSTRACT (Continuation of item 5 of the first sheet)**

The abstract is modified as follows:

line 17-19: Delete In the signal.....data processing";

# INTERNATIONAL SEARCH REPORT

International Application No
PCT/JP 00/06122

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11B20/18 H03M13/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11B H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A,P | US 6 003 151 A (CHUANG CHENG-TE)<br>14 December 1999 (1999-12-14)<br>abstract; figures 1,6,7<br>column 1, line 61 -column 4, line 19<br>column 5, line 51 -column 6, line 31<br>column 10, line 6 -column 12, line 24<br>column 15, line 3 - line 19 | 1-4 |
| A | PATENT ABSTRACTS OF JAPAN<br>vol. 1998, no. 10,<br>31 August 1998 (1998-08-31)<br>& JP 10 126279 A (MATSUSHITA ELECTRIC IND CO LTD), 15 May 1998 (1998-05-15)<br>abstract | 1,2 |

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 27 November 2000 | 04/12/2000 |

| Name and mailing address of the ISA | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL – 2280 HV Rijswijk<br>Tel. (+31–70) 340–2040, Tx. 31 651 epo nl,<br>Fax: (+31–70) 340–3016 | Schiwy-Rausch, G |

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Form PCT/ISA/210 (second sheet) (July 1992)

# INTERNATIONAL SEARCH REPORT

International Application No
PCT/JP 00/06122

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication,where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | PATENT ABSTRACTS OF JAPAN<br>vol. 1997, no. 08,<br>29 August 1997 (1997-08-29)<br>& JP 09 091889 A (MATSUSHITA ELECTRIC IND CO LTD), 4 April 1997 (1997-04-04)<br>abstract | 1-3 |
| A | EP 0 939 403 A (MATSUSHITA ELECTRIC IND CO LTD) 1 September 1999 (1999-09-01)<br>column 2, line 16 - line 47<br>column 3, line 3 - line 33<br>column 17, line 17 -column 20, line 35<br>figures 4-8 | 1,2 |
| A | PATENT ABSTRACTS OF JAPAN<br>vol. 1997, no. 09,<br>30 September 1997 (1997-09-30)<br>& JP 09 139026 A (MITSUBISHI ELECTRIC CORP), 27 May 1997 (1997-05-27)<br>abstract | 1,4 |
| A | PATENT ABSTRACTS OF JAPAN<br>vol. 1999, no. 11,<br>30 September 1999 (1999-09-30)<br>& JP 11 168392 A (TOSHIBA CORP),<br>22 June 1999 (1999-06-22) | |

1

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/JP 00/06122

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| US 6003151 A | 14-12-1999 | NONE | |
| JP 10126279 A | 15-05-1998 | NONE | |
| JP 09091889 A | 04-04-1997 | NONE | |
| EP 0939403 A | 01-09-1999 | CN 1233053 A<br>JP 11338723 A | 27-10-1999<br>10-12-1999 |
| JP 09139026 A | 27-05-1997 | NONE | |
| JP 11168392 A | 22-06-1999 | NONE | |

# PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

## PCT

To:
HAYASE, Kenichi
Hayase & Co. Patent Attorneys
8F, Esaka ANA Bldg.
17-1, Minoki-cho
Suita-shi
Osaka 564-0053
JAPON



**NOTICE INFORMING THE APPLICANT OF THE COMMUNICATION OF THE INTERNATIONAL APPLICATION TO THE DESIGNATED OFFICES**

(PCT Rule 47.1(c), first sentence)

| | |
|---|---|
| **Date of mailing** (day/month/year)<br>22 March 2001 (22.03.01) | |
| **Applicant's or agent's file reference**<br>P23070-PO | **IMPORTANT NOTICE** |
| **International application No.**<br>PCT/JP00/06122 | **International filing date** (day/month/year)<br>08 September 2000 (08.09.00) |
| **Priority date** (day/month/year)<br>10 September 1999 (10.09.99) | |
| **Applicant**<br>MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. et al | |

1. Notice is hereby given that the International Bureau has communicated, as provided in Article 20, the international application to the following designated Offices on the date indicated above as the date of mailing of this Notice:
   KR,US

   In accordance with Rule 47.1(c), third sentence, those Offices will accept the present Notice as conclusive evidence that the communication of the international application has duly taken place on the date of mailing indicated above and no copy of the international application is required to be furnished by the applicant to the designated Office(s).

2. The following designated Offices have waived the requirement for such a communication at this time:
   CN,ID,JP,SG

   The communication will be made to those Offices only upon their request. Furthermore, those Offices do not require the applicant to furnish a copy of the international application (Rule 49.1(a-bis)).

3. Enclosed with this Notice is a copy of the international application as published by the International Bureau on
   22 March 2001 (22.03.01) under No. WO 01/20607

### REMINDER REGARDING CHAPTER II (Article 31(2)(a) and Rule 54.2)

If the applicant wishes to postpone entry into the national phase until 30 months (or later in some Offices) from the priority date, **a demand for international preliminary examination** must be filed with the competent International Preliminary Examining Authority before the expiration of 19 months from the priority date.

It is the applicant's sole responsibility to monitor the 19-month time limit.

Note that only an applicant who is a national or resident of a PCT Contracting State which is bound by Chapter II has the right to file a demand for international preliminary examination.

### REMINDER REGARDING ENTRY INTO THE NATIONAL PHASE (Article 22 or 39(1))

If the applicant wishes to proceed with the international application in the **national phase**, he must, within 20 months or 30 months, or later in some Offices, perform the acts referred to therein before each designated or elected Office.

For further important information on the time limits and acts to be performed for entering the national phase, see the Annex to Form PCT/IB/301 (Notification of Receipt of Record Copy) and Volume II of the PCT Applicant's Guide.

| | |
|---|---|
| **The International Bureau of WIPO**<br>**34, chemin des Colombettes**<br>**1211 Geneva 20, Switzerland** | Authorized officer<br>J. Zahra |
| Facsimile No. (41-22) 740.14.35 | Telephone No. (41-22) 338.83.38 |

3897677

Form PCT/IB/308 (July 1996)

# PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

## PCT

**NOTIFICATION CONCERNING SUBMISSION OR TRANSMITTAL OF PRIORITY DOCUMENT**

(PCT Administrative Instructions, Section 41)

To:

C HAYASE, Kenichi
Hayase & Co. Patent Attorneys
8F, Esaka ANA Bldg.
17-1, Enoki-cho
Suita-shi
Osaka 564-0053
JAPAN



| | |
|---|---|
| Date of mailing (day/month/year)<br>02 November 2000 (02.11.00) | |
| Applicant's or agent's file reference<br>P23070-PO | **IMPORTANT NOTIFICATION** |
| International application No.<br>PCT/JP00/06122 | International filing date (day/month/year)<br>08 September 2000 (08.09.00) |
| International publication date (day/month/year)<br>Not yet published | Priority date (day/month/year)<br>10 September 1999 (10.09.99) |
| Applicant<br>MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. et al | |

1. The applicant is hereby notified of the date of receipt (except where the letters "NR" appear in the right-hand column) by the International Bureau of the priority document(s) relating to the earlier application(s) indicated below. Unless otherwise indicated by an asterisk appearing next to a date of receipt, or by the letters "NR", in the right-hand column, the priority document concerned was submitted or transmitted to the International Bureau in compliance with Rule 17.1(a) or (b).

2. This updates and replaces any previously issued notification concerning submission or transmittal of priority documents.

3. An **asterisk(*)** appearing next to a date of receipt, in the right-hand column, denotes a priority document submitted or transmitted to the International Bureau but not in compliance with Rule 17.1(a) or (b). In such a case, **the attention of the applicant is directed** to Rule 17.1(c) which provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

4. The **letters "NR"** appearing in the right-hand column denote a priority document which was not received by the International Bureau or which the applicant did not request the receiving Office to prepare and transmit to the International Bureau, as provided by Rule 17.1(a) or (b), respectively. In such a case, **the attention of the applicant is directed** to Rule 17.1(c) which provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

| Priority date | Priority application No. | Country or regional Office or PCT receiving Office | Date of receipt of priority document |
|---|---|---|---|
| 10 Sept 1999 (10.09.99) | 11/256736 | JP | 27 Octo 2000 (27.10.00) |

**The International Bureau of WIPO**
**34, chemin des Colombettes**
**1211 Geneva 20, Switzerland**

Facsimile No. (41-22) 740.14.35

Authorized officer

S. Mandallaz

Telephone No. (41-22) 338.83.38